

Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A data processing device configured according to a device configuration so as to be capable of executing a program comprising an instruction, the device comprising

 a configurable functional unit for executing the instruction according to a configurable function that is configured outside the instruction,

 the configurable functional unit having including:

 [[-]] a unit input and a unit output for inputting and outputting a plurality of bits of an operand and a result to a one or more source and destination registers specified by the instruction, respectively, the configurable function unit comprising
 a unit output for outputting a plurality of bits of a result to a destination register specified by the instruction,

 [[-]] a plurality of independent configurable logic blocks for performing programmable logic operations to implement the configurable function and producing outputs having a first relative order of bits;

 [[-]] a first programmable connection circuit between the unit input and the logic blocks, for selectively coupling inputs of the logic blocks to bits from the unit input, dependent on the configured function;

 [[-]] a second programmable connection circuit between the logic blocks and the unit output, for selectively coupling bits of the unit output to outputs of the logic blocks to the unit output in a second order of bits, dependent on the configured function; wherein, for at least one configured function, the second programmable connection circuit reverses the relative order of outputs of different logic blocks.

2. (Currently amended) A-The data processing device according to Claim of claim 1, each logic block having a plurality of outputs, at least one of the bits of the unit output being connectable exclusively to one of the outputs of each logic block, the second programmable connection circuit comprising a multiplexer for coupling the one of the outputs of a selected one of the logic blocks to the at least one of the bits of the unit output.
3. (Currently amended) A-The data processing device according to Claim of claim 2, each logic block having a plurality of outputs, each of the bits of the unit being connectable exclusively to a respective one of the outputs of each logic block, the second programmable connection circuit comprising a respective multiplexer for each particular bit of the unit output, for coupling the respective one of the outputs of a selected one of the logic blocks to the particular bit of the unit output.
4. (Currently amended) A-The data processing device according to Claim of claim 1, either the first programmable connection circuit or the second programmable connection circuit having a fixed, unprogrammable connection to an input or output of one of the independent configurable logic blocks and a programmable connection to a remainder of the inputs and outputs.

5. (Currently amended) A method of programming a configurable processing device according to a device configuration to perform a processing task, wherein the device ~~has~~includes a configurable processing unit that ~~comprises several~~includes one or more programmable logic blocks, the method comprising:

[[[-]]] identifying a special complex of operations that occurs in the task and requires ~~an~~one or more operand data words and produces a result data word;

[[[-]]] searching for an assignment of the logic operations for producing different bits of the result data word to different ones of the programmable logic blocks, so that the logic operations for producing a subset of the bits of the result data word that, if implemented together in one of the programmable logic blocks, would exceed the capacity of that one of the programmable logic blocks, are distributed over different ones of the logic blocks;

[[[-]]] programming each of the programmable logic blocks to perform the logic operations for the bits of the result data word assigned to it;

[[[-]]] programming connection circuits in from of the programmable logic blocks and subsequent to the logic blocks so as to perform a first routing of bits of an operand of a special instruction to the programmable logic blocks that use those bits of the operand in the logic operations and so as to perform a second routing outputs of the programmable logic blocks to bits of the result data word to which the programmable logic blocks are assigned;

~~wherein, for at least one configured function, a relative order of outputs of different logic blocks is reversed during said second routing.~~

6. (Currently amended) A method of executing a program with a processing device with a configurable functional unit according to a device configuration, the method comprising ~~executing the following steps in response to a configurable instruction:~~

[[[-]]] inputting one or more words ~~bits of an~~ one or more ~~operands~~ of the configurable instruction into the configurable functional unit, each word including a plurality of bits;

[[[-]]] selectively coupling the bits of the words of the operands to inputs of logic blocks, dependent on a configured function;

[[[-]]] performing programmable logic operations to implement the configurable function to provide an output word that includes a plurality of bits;

[[[-]]] selectively coupling bits of the output word ~~outputs of the logic blocks~~ to bits of a result word, dependent on a configured function; ~~wherein, for at least one configured function, a relative order of outputs of different logic blocks is reversed during said selectively coupling outputs.~~

7. (New) A data processing device comprising:

a register file that includes a plurality of registers, each register including a word, each word including a plurality of bits in a first bit order, and
at least one configurable function units that is dynamically configurable to effect different functions at different times, based on received configuration data, the at least one configurable function unit including:

a first connection circuit that is configured to receive one or more words from the plurality of registers, and to provide one or more words of bits in a second bit order based on the received configuration data,

one or more programmable logic blocks that are configured to receive the one or more words in the second bit order from the first connection circuit, and to provide an output word of bits in a first output bit order based on the received configuration data,

a second connection circuit that is configured to receive the output word and to provide therefrom a word of bits in a second output bit order that is stored in a destination register of the plurality of registers based on the received configuration data.

8. (New) The data processing device of claim 7, including

an input unit that is configured to receive the one or more words from the plurality of registers, and to provide the one or more words to the first connection circuit.

9. (New) The data processing device of claim 8, including

an output unit that is configured to receive the one or more words from the second connection circuit, and to provide the one or more words to the destination register.

10. (New) The data processing device of claim 7, including

an output unit that is configured to receive the one or more words from the second connection circuit, and to provide the one or more words to the destination register.

11. (New) The data processing device of claim 7, wherein

source registers of the one or more words from the plurality of registers are identified in an instruction that effects execution of a current function of the at least one configurable function unit.

12. (New) The data processing device of claim 7, wherein

the destination register is identified in the instruction.

13. (New) A device comprising:

a processor that is configured to execute instructions that identify: an operation, one or more source registers, and a destination register, each register including a word that includes a plurality of bits, the processor including:

a first connection circuit that receives a word from a source register of the one or more source registers and provides an operand word that includes a plurality of bits that are arranged in a bit order based on a programmed set of configuration data corresponding to the operation,

a configurable function circuit that provides a result word based on the operand word and the programmed set of configuration data,

a second connection circuit that receives the result word and provides an output word for storing in the destination register that includes a plurality of bits that are arranged in a bit order based on the programmed set of configuration data.

14. (New) The device of claim 13, wherein the processor includes

an input port that is configured to receive the word from the source register, and to provide the word to the first connection circuit.

15. (New) The device of claim 14, wherein the processor includes
an output port that is configured to receive the output word from the second connection circuit, and to provide the output word to the destination register.
16. (New) The device of claim 13, wherein the processor includes
an output port that is configured to receive the output word from the second connection circuit, and to provide the output word to the destination register.
17. (New) The device of claim 13, wherein the processor includes
one or more other function circuits that are configured to receive one or more words from the plurality of registers and provide one or more other result words to the plurality of registers.
18. (New) The device of claim 13, including
an instruction issue unit that is configured to provide the instructions to the processor.
19. (New) The device of claim 18, including
a configuration control circuit that is configured to provide the set of configuration data corresponding to the operand based on a configuration instruction from the instruction issue unit.
20. (New) The device of claim 13, including
a configuration control circuit that is configured to provide the set of configuration data corresponding to the operand.